3 通道同步降压整合型开关电源转换器

EA3059C

规格书

概述

EA3059C是一款整合了3通道同步降压电路的整合型开关电源转换器，适合5V适配器输入及单颗锂电池输入之应用。其输入电压范围为2.7V至5.5V，无论是在轻载或重载之工作环境下皆能提供很高的输出效率。EA3059C内置3通道功率开关管和同步整流开关管以及内部补偿线路，能够减少外围元器件进而降低设计成本，各自独立的致能控制脚能够提供各通道电源启动时序安排的最大灵活性。EA3059C使用24 pin QFN 4mm x 4mm封装，能够提供最佳散热性及减少PCB板面积。

特性

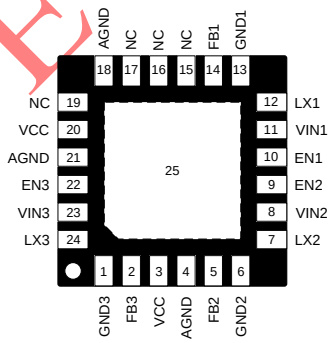
- 2.7V 至 5.5V 输入电压范围
- 3通道降压转换器
  - 可调输出电压范围 0.6V 至输入电压
  - 通道1/通道2/通道3 最大持续工作电流： 3A/2A/2A (3通道总输出功率需低于10W)
  - 通道1/通道2/通道3 最大瞬间负载电流： 3.5A/2.5A/2.5A
  - 180° 开关相位差架构
  - 恒定开关频率1.5MHz
  - 允许低压差工作，占空比高达100%
  - 独立致能脚位控制
  - 内置补偿线路
  - 逐周期电流限制保护
  - 短路保护
- 自动回复过温保护
- 24-pin 4mm x 4mm QFN 封装

应用

- 机顶盒
- 智能型手机
- 无线路由器

脚位图

(上视图)



QFN 4x4-24

脚位定义

脚位名	功能描述	脚位号
GND3	Power ground pin of CH3.	1
FB3	Feedback input of CH3. Connect to output voltage with a resistor divider.	2
VCC	Input supply pin for internal control circuit.	3, 20
AGND	Analog ground pin.	4, 18, 21
FB2	Feedback input of CH2. Connect to output voltage with a resistor divider.	5
GND2	Power ground pin of CH2.	6
LX2	Internal MOSFET switching output of CH2. Connect LX2 pin with a low pass filter circuit to obtain a stable DC output voltage.	7
VIN2	Power input pin of CH2. Recommended to use a 10uF MLCC capacitor between VIN2 pin and PGND2 pin.	8
EN2	CH2 turns on/turns off control input. Don't leave this pin floating.	9
EN1	CH1 turns on/turns off control input. Don't leave this pin floating.	10
VIN1	Power input pin of CH1. Recommended to use a 10uF MLCC capacitor between VIN1 pin and PGND1 pin.	11
LX1	Internal MOSFET switching output of CH1. Connect LX1 pin with a low pass filter circuit to obtain a stable DC output voltage.	12
GND1	Power ground pin of CH1.	13
FB1	Feedback input of CH1. Connect to output voltage with a resistor divider.	14
NC	No connect.	15, 16, 17, 19
EN3	CH3 turns on/turns off control input. Don't leave this pin floating.	22
VIN3	Power input pin of CH3. Recommended to use a 10uF MLCC capacitor between VIN3 pin and PGND3 pin.	23
LX3	Internal MOSFET switching output of CH3. Connect LX3 pin with a low pass filter circuit to obtain a stable DC output voltage.	24
Exposed Pad	The Exposed Pad must be soldered to a large PCB copper plane and connected to GND for appropriate dissipation.	25

内部架构框图

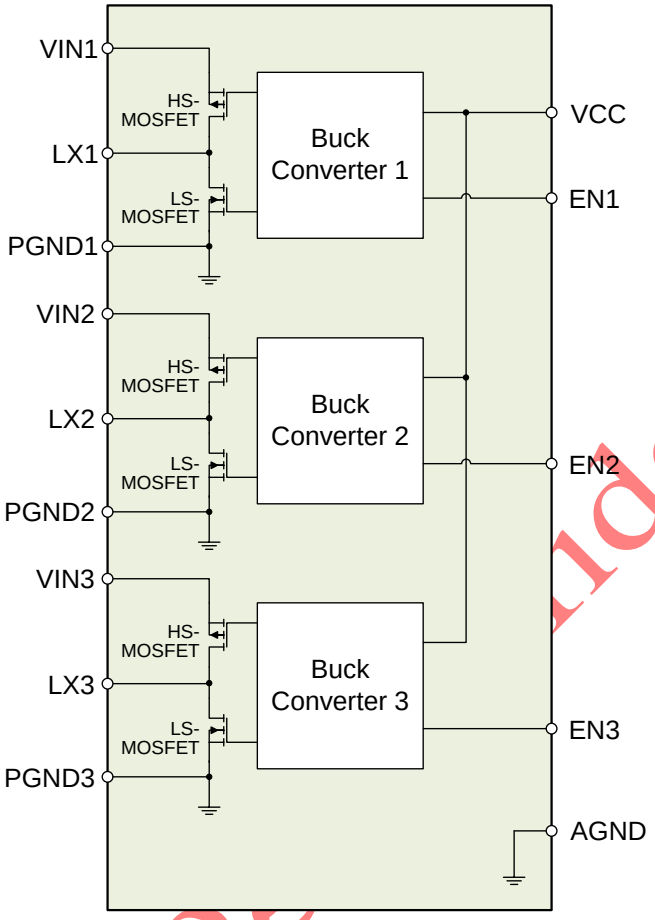


图 1. EA3059C 内部功能模块框图

绝对最大额定参数

参数	范围
Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}, V_{VCC})	-0.3V to +6.5V
LX Pin Voltage (V_{LX1}, V_{LX2}, V_{LX3})	-0.3V to V_{VINX}+0.3V
All Other Pins Voltage	-0.3V to +6.5V
Ambient Temperature operating Range (T_A)	-40°C to +85°C
Maximum Junction Temperature (T_{Jmax})	+150°C
Lead Temperature (Soldering, 10 sec)	+260°C
Storage Temperature Range (T_S)	-65°C to +150°C

Note (1):Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability and lifetime.

封装热特性

参数	数值
QFN 4x4-24 Thermal Resistance (θ_{JC})	7.5°C/W
QFN 4x4-24 Thermal Resistance (θ_{JA})	50°C/W
QFN 4x4-24 Power Dissipation at T_A=25°C (P_{Dmax})	2.5W

Note (1): P_{Dmax} is calculated according to the formula: $P_{DMAX}=(T_{JMAX}-T_A)/\theta_{JA}$.

建议工作条件

参数	范围
Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}, V_{VCC})	+2.7V to +5.5V
Junction Temperature Range (T_J)	-40°C to +125°C

电气特性

V_{VINX}=3.6V, V_{VCC}=3.6V, T_A=25°C, unless otherwise noted

参数	符号	测试条件	最小值	典型值	最大值	单位
Input Supply Voltage						
Input Voltage	V_{INX}		2.7		5.5	V
Control Circuit Input Voltage	V_{VCC}		2.7		5.5	V
Buck Regulator 1						
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		0.1	1	uA
Quiescent Current	I_Q	Non-switching, No Load		40	80	uA
UVLO Threshold	V_{UVLO}	V_{VIN} Rising	1.9	2.1	2.3	V
UVLO Hysteresis	$V_{UV-HYST}$			0.1		V
Output Load Current	I_{LOAD}				3	A
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
Switching Frequency	F_{SW}	I_{LOAD} = 100mA	1	1.5	2	MHz
Short Frequency	$F_{SW-SHORT}$	V_{OUT} = 0V		300		KHz
PMOS Current Limit	I_{LIM-P}		4	5		A
PMOS On-Resistance	$R_{DS(ON)-P}$	I_{LOAD} = 100mA		90		mΩ
NMOS On-Resistance	$R_{DS(ON)-N}$	I_{LOAD} = 100mA		85		mΩ
Enable Pin Input Low Voltage	V_{EN-L}				0.4	V
Enable Pin Input High Voltage	V_{EN-H}		2			V
Maximum Duty Cycle	D_{MAX}		100			%
Buck Regulator 2, 3						
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		0.1	1	uA
Quiescent Current	I_Q	Non-switching, No Load		40	80	uA
UVLO Threshold	V_{UVLO}	V_{VIN} Rising	1.9	2.1	2.3	V
UVLO Hysteresis	$V_{UV-HYST}$			0.1		V
Output Load Current	I_{LOAD}				2	A
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
Switching Frequency	F_{SW}	I_{LOAD} = 100mA	1	1.5	2	MHz

电气特性

V_{VINX}=3.6V, V_{VCC}=3.6V, T_A=25°C, unless otherwise noted

参数	符号	测试条件	最小值	典型值	最大值	单位
Short Frequency	$F_{SW-SHORT}$	V_{OUT} = 0V		300		KHz
PMOS Current Limit	I_{LIM-P}		4	5		A
PMOS On-Resistance	$R_{DS(ON)-P}$	I_{LOAD} = 100mA		100		mΩ
NMOS On-Resistance	$R_{DS(ON)-N}$	I_{LOAD} = 100mA		90		mΩ
Enable Pin Input Low Voltage	V_{EN-L}				0.4	V
Enable Pin Input High Voltage	V_{EN-H}		2			V
Maximum Duty Cycle	D_{MAX}		100			%
Thermal Shutdown						
Thermal Shutdown Threshold	T_{OTP}			165		°C
Thermal Shutdown Hysteresis	T_{HYST}			30		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
(2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

应用线路参考

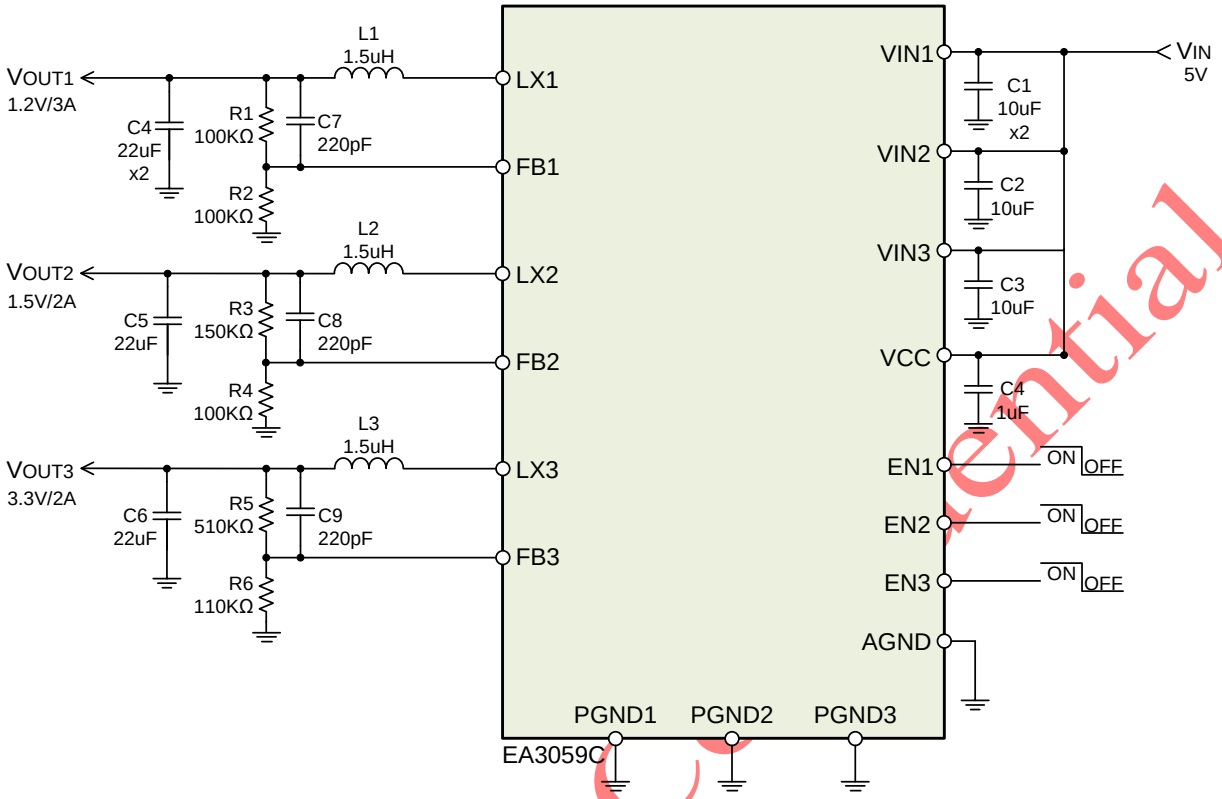


图 2. 典型应用线路图

订货需知

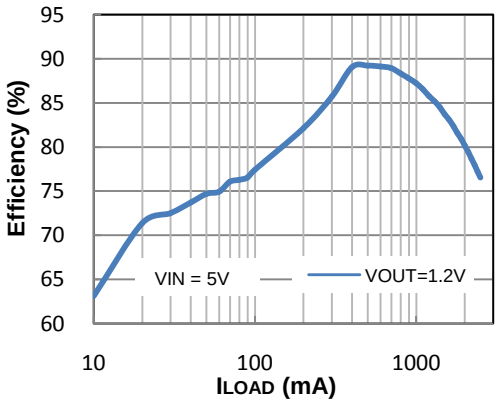
型号	封装	包装
EA3059CQDR	QFN 4mm x 4mm-24	Tape & Reel / 3000

Note (1):"QD": Package type code.
(2):"R": Tape & Reel.

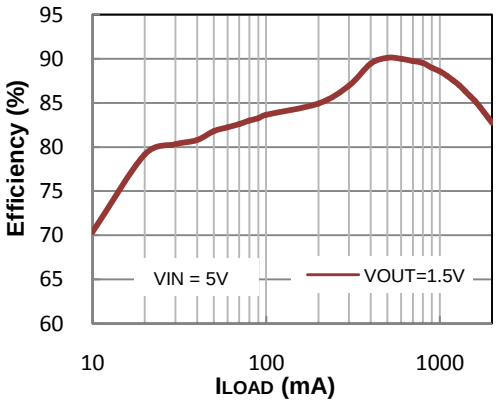
性能测试

V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.2V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, L1=1.5uH, L2=1.5uH, L3=1.5uH, T_A=25°C, unless otherwise noted

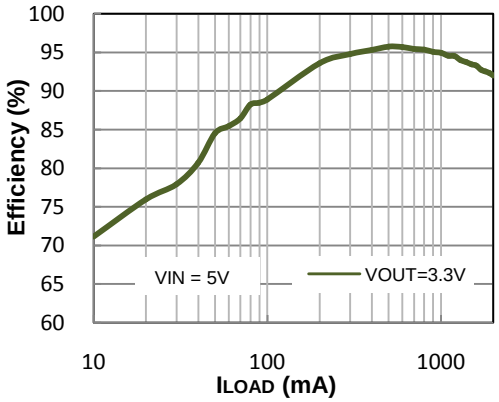
Efficiency vs. Load Current



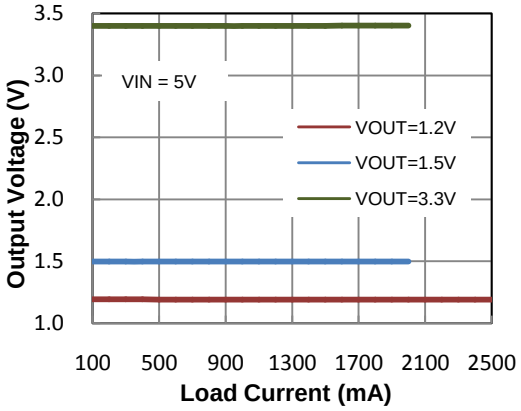
Efficiency vs. Load Current



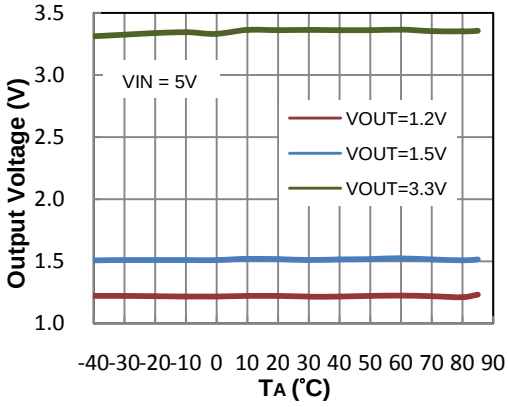
Efficiency vs. Load Current



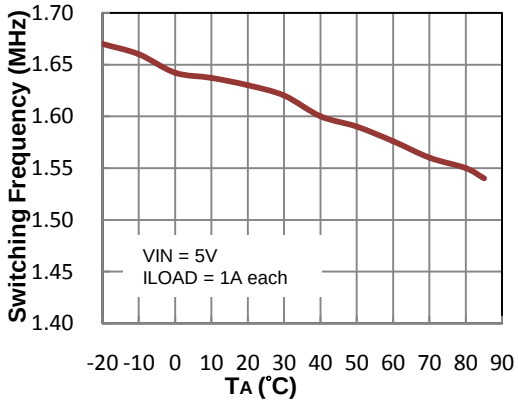
Load Regulation



VOUT vs. Ambient Temp.

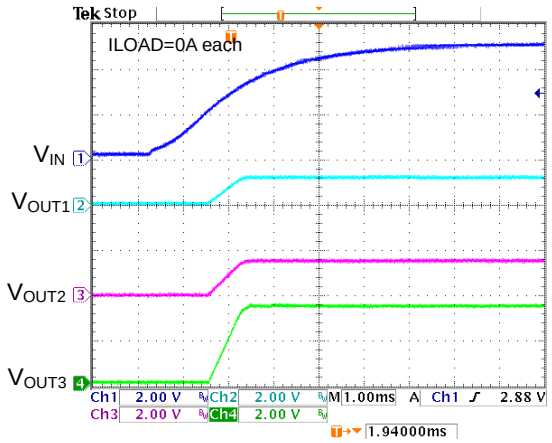


Freq. vs. Ambient Temp.

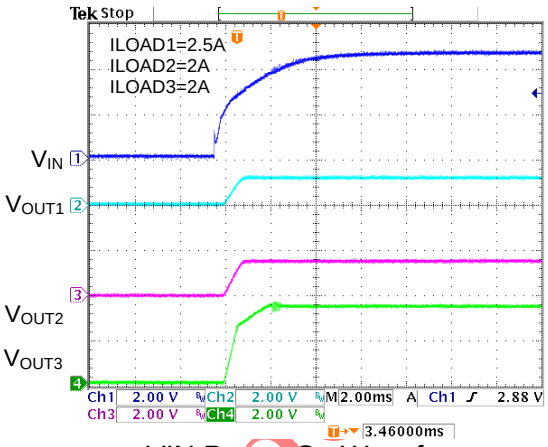


性能测试

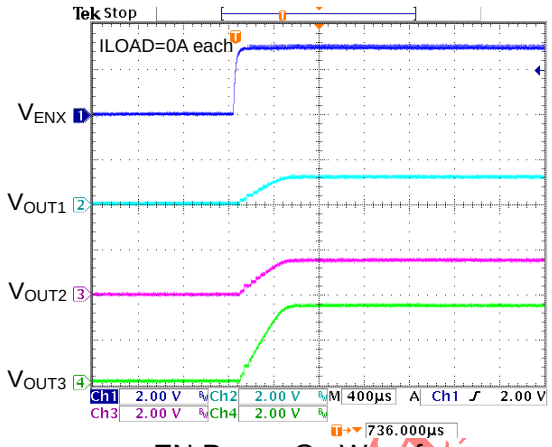
V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.2V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, L1=1.5uH, L2=1.5uH, L3=1.5uH, T_A=25°C, unless otherwise noted



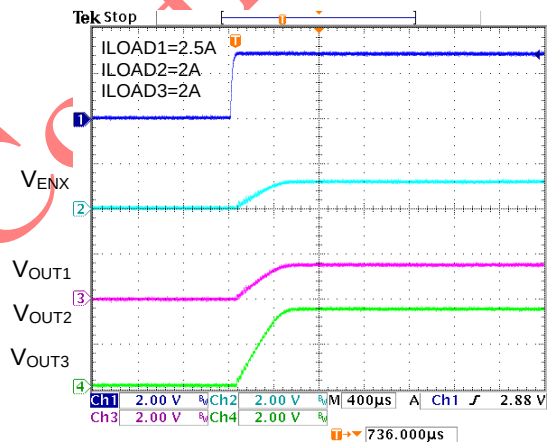
VIN Power On Waveform



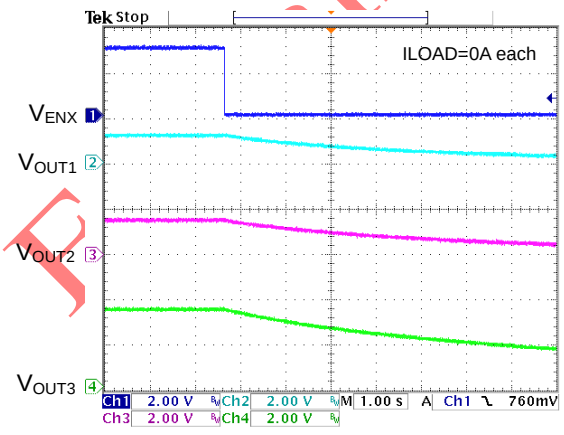
VIN Power On Waveform



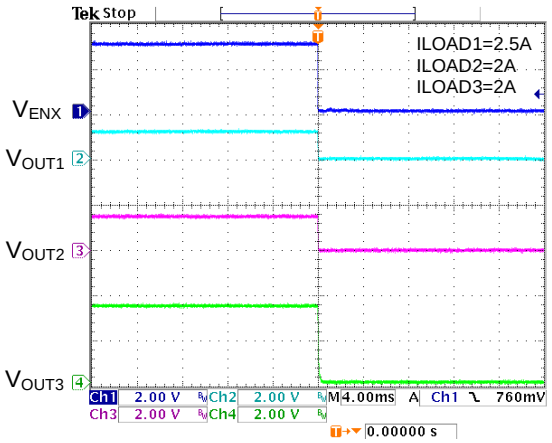
EN Power On Waveform



EN Power On Waveform



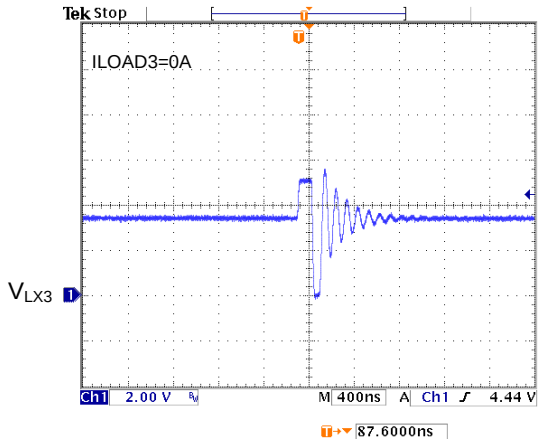
EN Power Off Waveform



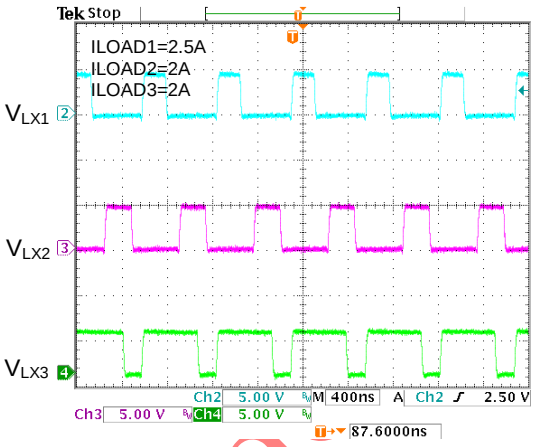
EN Power Off Waveform

性能测试

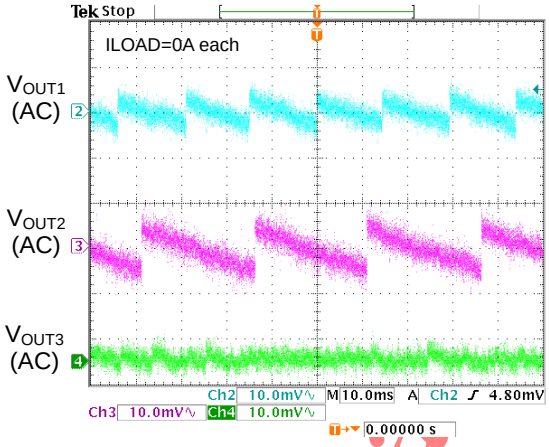
V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.2V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, L1=1.5uH, L2=1.5uH, L3=1.5uH, T_A=25°C, unless otherwise noted



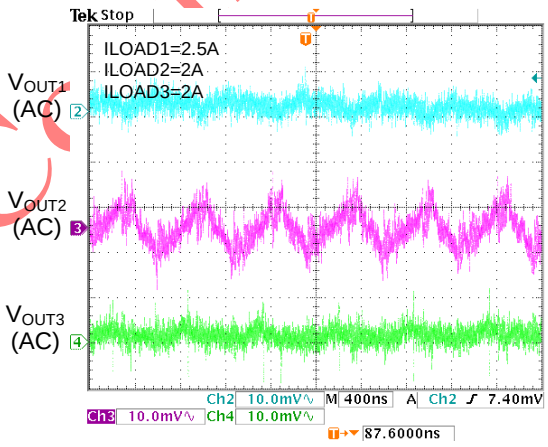
V_{LX3} Switching Waveform



$V_{LX1,2,3}$ Switching Waveform



Output Ripple Waveform



Output Ripple Waveform

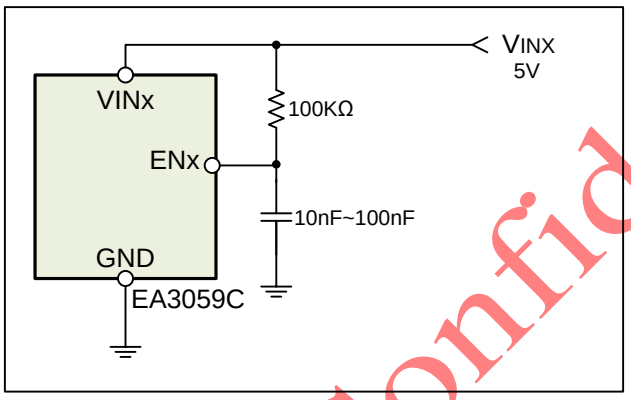
功能描述

PFM/PWM Operation

Each of the buck regulators can be operated at PFM/PWM mode. If the output current is less than 150mA (typ.), the regulators automatically enters the PFM mode. The output voltages and output ripples at PFM mode are higher than the output voltages and output ripples at PWM mode. But at very light load, the PFM mode operation provides higher efficiency than PWM mode operation.

Enable Control

The EA3059C is a high efficiency Power Management IC which is designed for IPC applications. It incorporates three 1A synchronous buck regulators and can be controlled by individual EN pins. The start-up time for each channel can be programmed by using the circuit shown as below:



180° Phases Shifted Architecture

In order to reduce the input ripple current, the EA3059C applied 180° phases shifted architecture. Buck1 and Buck3 have the same phase and Buck2 is 180° out of phase. This architecture allows the system board has less ripple current, and thus can reduce EMI.

Over Current Protection

The EA3059C internal three regulators have their own cycle-by-cycle current limit circuits. When the inductor peak current exceeds the current limit threshold, the output voltage starts to drop until FB pin voltage is below the threshold, typically 30% below the reference. Once the threshold is triggered, the switching frequency is reduced to 300KHz (typ.).

Thermal Shutdown

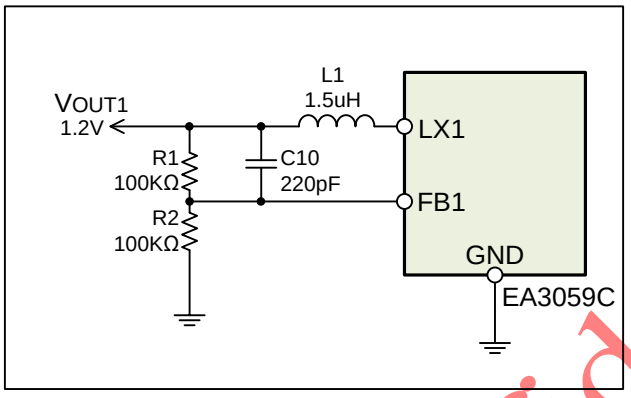
The EA3059C will automatically disabled if the die temperature is higher than the thermal shutdown threshold point. To avoid unstable operation, the hysteresis of thermal shutdown is about 30°C.

使用说明

Output Voltage Setting

Each of the regulators output voltage can be set via a resistor divider (ex. R1, R2). The output voltage is calculated by following equation:

$$V_{OUT1} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$



The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

输出电压	分压电阻 R1	分压电阻 R2	精度
3.3V	510KΩ	110KΩ	1%
1.8V	200KΩ	100KΩ	1%
1.5V	150KΩ	100KΩ	1%
1.2V	100KΩ	100KΩ	1%

Input / Output Capacitors Selection

The input capacitors are used to suppress the noise amplitude of the input voltage and provide a stable and clean DC input to the device. Because the ceramic capacitor has low ESR characteristic, so it is suitable for input capacitor use. It is recommended to use X5R or X7R MLCC capacitors in order to have better temperature performance and smaller capacitance tolerance. In order to suppress the output voltage ripple, the MLCC capacitor is also the best choice. The suggested part numbers of input / output capacitors are as follows:

厂商	型号	容值	耐压值	特性参数	尺寸
TDK	C2012X5R1A106M	10uF	10V	X5R	0805
TDK	C3216X5R1A106M	10uF	10V	X5R	1206
TDK	C2012X5R1A226M	22uF	10V	X5R	0805
TDK	C3216X5R1A226M	22uF	10V	X5R	1206

Output Inductor Selection

The output inductor selection mainly depends on the amount of ripple current through the inductor ΔI_L. Large ΔI_L will cause larger output voltage ripple and loss, but the user can use a smaller inductor to save cost and space. On the contrary, the larger inductance can get smaller ΔI_L and

thus the smaller output voltage ripple and loss. But it will increase the space and the cost. The inductor value can be calculated as:

$$L = \frac{V_{PWR} - V_{OUT}}{\Delta I_L \times F_{SW}} \times \frac{V_{OUT}}{V_{PWR}}$$

For most applications, 1.0uH to 2.2uH inductors are suitable for EA3059C.

Power Dissipation

The total output power dissipation of EA3059C should not to exceed the maximum 6W range. The total output power dissipation can be calculated as:

$$P_{D(total)} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3}$$

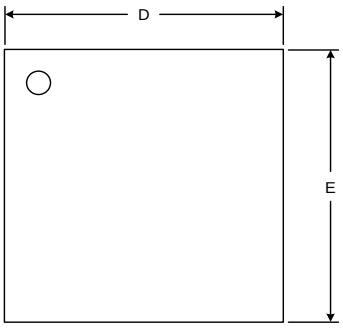
PCB Layout Recommendations

Layout is very critical for PMIC designs. For EA3059C PCB layout considerations, please refer to the following suggestions to get best performance.

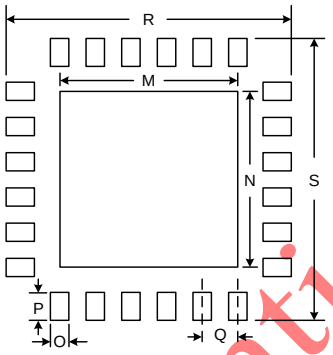
- It is suggested to use 4-layer PCB layout and place LX plane and output plane on the top layer, place VIN plane in the inner layer.
- The top layer SMD input and output capacitors ground plane should be connected to the internal ground layer and bottom ground plane individually by using vias.
- The AGND should be connected to inner ground layer directly by using via.
- High current path traces need to be widened.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.
- Keep the feedback path (from V_{OUTX} to FBx) away from the noise node (ex. LXx). LXx is a high current noise node. Complete the layout by using short and wide traces.
- The top layer exposed pad ground plane should be connected to the internal ground layer and bottom ground plane by using a number of vias to improve thermal performance.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.

封装讯息

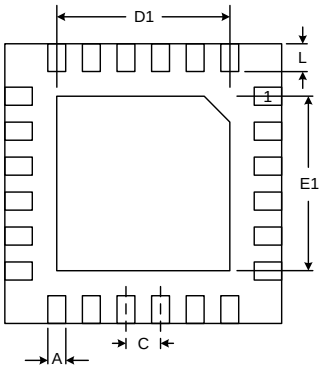
QFN 4mm x 4mm-24 Package



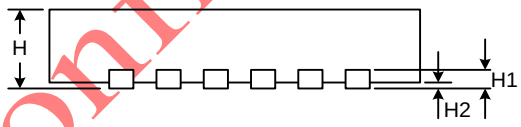
Top View



Recommended Layout Pattern



Bottom View



Side View

Unit: mm

符号	尺寸 最小值	最大值	符号	尺寸 典型值
A	0.18	0.30	M	2.60
C	0.45	0.55	N	2.60
D	3.95	4.05	O	0.30
E	3.95	4.05	P	0.80
D1	2.30	2.70	Q	0.50
E1	2.30	2.70	R	4.70
L	0.35	0.45	S	4.70
H	0.70	0.90		
H1	0.17	0.25		
H2	0.00	0.05		